6.6 A Fully Integrated UWB PHY in 0.13μm CMOS

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The WiMedia Alliance has proposed an UWB OFDM system with data rates from 53.3 to 480Mbps operating in the 3.1 to 10.6GHz band [1]. These data rates are comparable to wired specifications, such as USB 2.0, enabling many applications developed for wired platforms to migrate to this wireless technology. However, many of these products require compact and low-cost hardware platforms. Therefore, highly integrated all-CMOS SoCs may offer competitive advantages for UWB applications when compared with other less integrated approaches. We present an integrated RF transceiver and digital PHY on a single CMOS chip that includes all the active circuitry required for operation in Band Group #1 (3.1 to 4.8GHz), and supports both fixed-frequency and frequency-hopping modes in 528MHz bands.

A block diagram of the complete SoC is shown in Fig. 6.6.1. Details of the direct-conversion RF transceiver are given below. In receive mode, the I and Q baseband signals are digitized at 528MS/s by 5b ADCs. The packet detection and frame synchronization sequence is detected, and appropriate gain settings are provided to the RF transceiver. Channel estimation, phase tracking, and signal demapping are performed after transformation by a 128-point FFT. Different data rates are implemented through variations in the coding rate, coding type, and modulation. Convolutional codes with rates of 1/3, 1/2, 5/8, and 3/4 are supported, along with dual-carrier modulation (DCM) and QPSK modulation. In addition, tone and symbol interleaving improve performance in fading channels. Soft decisions from the demapper are resolved by the Viterbi decoder and the decoded data are output at the MAC/PHY interface. For transmission, the process is reversed except that the I and Q signals sent to the 5b DACs are up-sampled to 1056MS/s. A clock generation circuit provides clock signals for the digital PHY and data converters. In the frequency-hopping mode, a band-select signal provides an indication to the RF transceiver of the appropriate operating frequency.

A block diagram of the direct-conversion RF transceiver is shown in Fig. 6.6.2. In order to enable agile frequency hopping, this design utilizes three separate RF blocks for each operating frequency in Band Group #1 [2]. Each block consists of a tuned amplifier stage, I/Q mixers, and integer-N frequency synthesizer. In frequency-hopping mode, the appropriate RF block is selected for each OFDM symbol, as indicated by the *Band Select* signal. Each mixer shares a common output connection to the RX baseband circuitry. Direct-conversion receivers are sensitive to LO carrier leakage. However, due to transistor frequency response and power consumption limitations, the VCOs in this design operate at the RF carrier frequency. To reduce LO leakage and other unwanted coupling, ring-oscillators have been employed instead of *LC*-based oscillators. In addition, 13 on-chip linear voltage regulators are employed to provide circuit isolation and further limit coupling through package bondwires. Each voltage regulator design has a programmable output voltage, requires no external components, and occupies 0.007mm^2. The receiver baseband circuitry comprises 5th-order channel selection filters, PGAs, RSSI circuitry, and dc offset compensation. The fast frequency-hopping in this system places additional constraints on the design of a direct-conversion receiver. AC coupling cannot be employed reliably because dc offsets are in part carrier-frequency dependent, and the fast settling requirement of 9ns in the system prevents resettling of ac-coupled circuitry. Furthermore, different frequency bands have different RF path loss parameters, resulting in different receiver gain settings. Therefore, any dc-offset correction must remain effective for different gain and carrier-frequency settings.

Figure 6.6.3 shows a more detailed schematic of one channel in the receiver baseband. Each stage consists of a differential amplifier with a zeroing function and a current-mode DAC. In this amplifier architecture, offsets appear as a current applied to the resistive loads R_L. Offset cancellation is accomplished through a corrective current provided by the DAC. Gain reduction is achieved through switch resistor R_D, so that the offset corrections are independent of gain. The receiver chain is calibrated through a digital circuit that measures the comparator output to determine the appropriate correction. Band-dependent offset correction of the RF mixers is accomplished by using three separate DACs and a high-speed analog MUX. Each frequency band is calibrated separately. DC offsets remain within design tolerances for temperature variations of ±50˚C and for all valid receiver gain settings.

The transmitter section employs many of the same concepts as the receiver for implementing frequency hopping. Figure 6.6.4 shows a simplified circuit diagram of the modulator circuit (one channel), and the shared switched-inductor load. Capacitors tuned with MOS switches result in high-Q tuning elements, but at the expense of additional parasitic capacitance at the output node. In this system, the 528MHz channel bandwidth makes the use of high-Q resonant circuits undesirable. The balanced switch configuration used in this design allows the use of a smaller switch for a given parasitic resistance. Furthermore, the parasitic capacitance of the switch is partially transformed by the inductor when referred to the output node. The use of switched inductors also allows each inductor to be optimized separately, potentially allowing a wider operating range than a single-inductor switched-capacitor method. In addition to this band-dependent tuning, the RF output power can be adjusted separately for each band. Figure 6.6.5 shows the transmitter output spectrum in frequency-hopping mode, after band-dependent power output correction.

The chip was implemented in a 1P8M digital 0.13μm CMOS process and packaged in a 64-pin QFN package with an exposed paddle. Figure 6.6.6 shows a micrograph of the chip. The die measures 3.4mm×5mm. Without precautions, the integration of RF and digital PHY circuitry could result in degraded system performance. In addition to employing on-chip voltage regulators, the RF transceiver is separated from the digital circuitry by a 50μm-wide path of substrate contacts that has a dedicated downbond. Digital grounds were bonded to dedicated package pins, allowing the PCB to have separate analog and digital ground planes. Figure 6.6.7 shows a table of the measured receiver sensitivity for various data rates, using 200-byte packets and a maximum packet error-rate of 8%. The RF transceiver draws 100mA in receive mode and 70mA in transmit mode.

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References:
[1] A. Batra et al., MultiBand OFDM Physical Layer Proposal, IEEE 802.15-03/268r4, Sept., 2004.
[2] B. Razavi et al., "A 0.13-μm CMOS UWB Transceiver," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb., 2005.

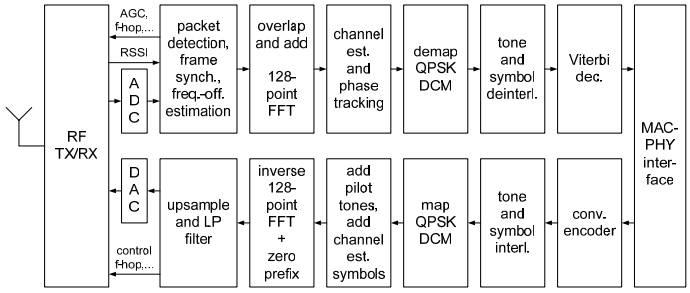

Figure 6.6.1: Block diagram of an integrated UWB OFDM PHY.

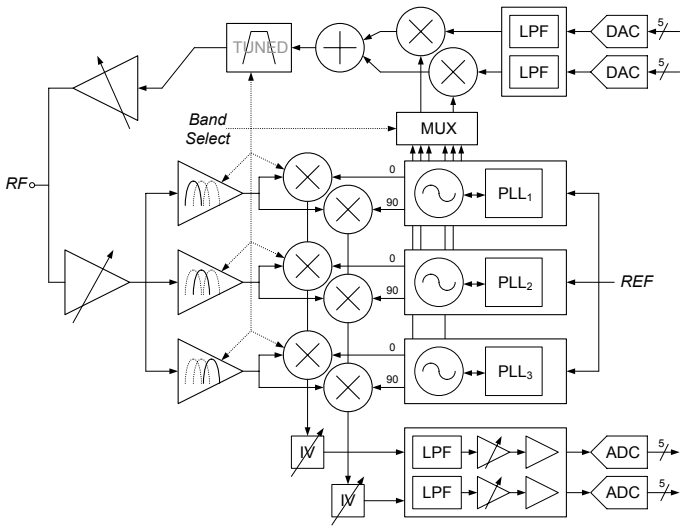

Figure 6.6.2: Block diagram of a direct-conversion transceiver.

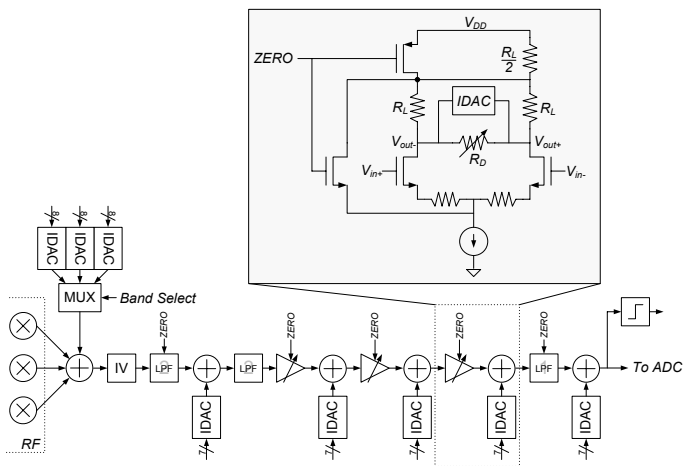

Figure 6.6.3: Block diagram of RX baseband (one channel, RSSI not shown).

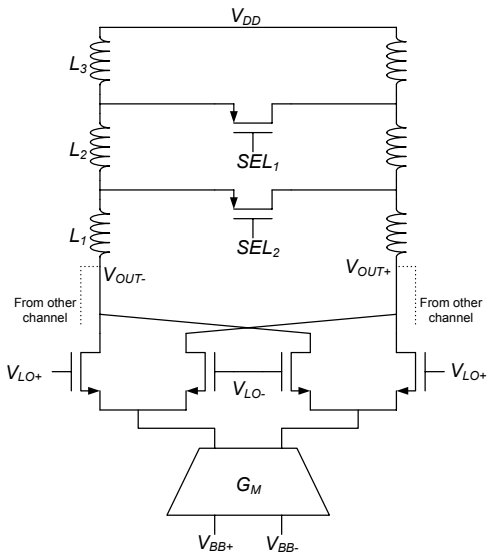

Figure 6.6.4: Simplified modulator circuit (one channel) and inductive load.

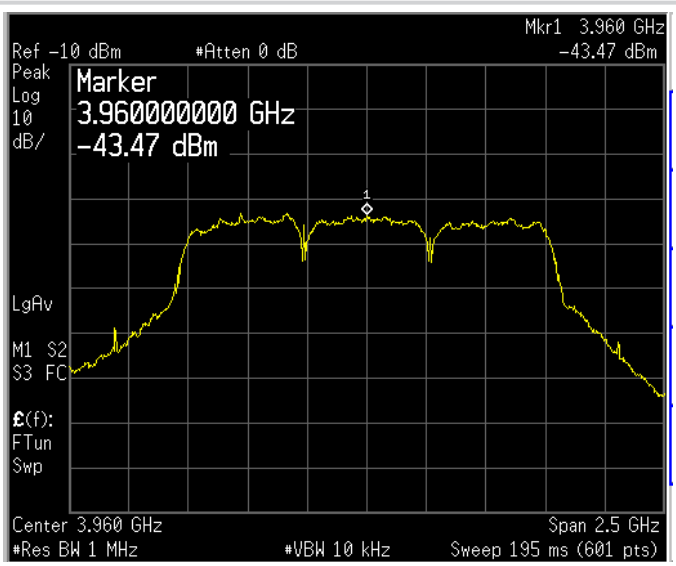

Figure 6.6.5: Transmit output spectrum in frequency-hopping mode.

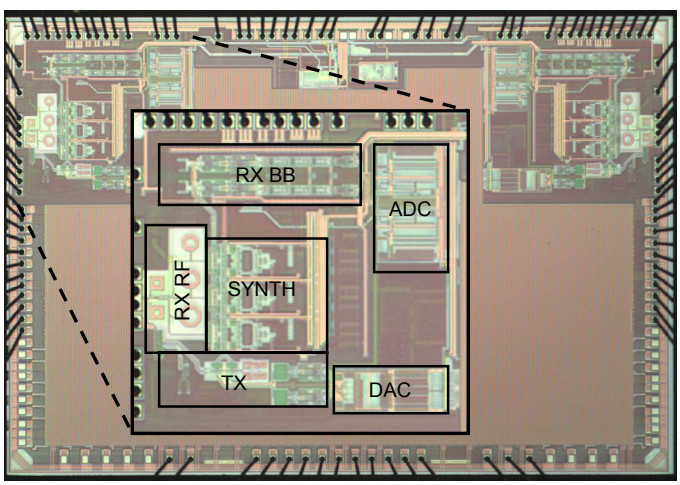

Figure 6.6.6: Chip micrograph.

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Data Rate (Mbps)	Receiver Sensitivity* (dBm)
53.3	-82
106.7	-80.5
200	-77.1
320	-75
480	-71.3

*Measured at 8% PER using 200-Byte packets

Figure 6.6.7: Measured receiver sensitivity versus data rate.

